# MULTI-PHASE CONVERTER WITH BALANCED CURRENTS

## CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Application No. 60/151,982, filed Sep. 1, 1999.

## FIELD OF THE INVENTION

The present invention relates to an apparatus and method for balancing the individual channel currents in a multi-phase DC/DC converter.

## DESCRIPTION OF THE RELATED ART

There are no known prior art devices or methods that specifically balance the channel currents of multi-phase converters.

Personal computers have direct current (DC) power supplies to regulate their operating voltage and current. Early personal computers operated their circuits at ±5 volts and drew several amps of current. In order to speed-up performance, operating voltages were dropped to the range of ±1.5 to 1.0 volts and currents have risen to 50 or more amps. It is more economical to provide the 50 or more amps from several power sources rather than from a single source. This has led many power supply manufacturers to provide multi-phase converters with two or more current channels. While there are more component parts in multi-phase systems, the parts themselves are smaller and typically less expensive than the high-power parts which must be used in a single-converter having similar current capabilities.

When multi-phase converters supply the same load there is often a voltage mismatch between the channels. If two or more channels have even slightly different output voltages, current will flow mostly from the channels with the highest voltage. Some converters have the ability to sink as well as source output current. In those converters, current may flow from one channel to another, regardless of load current. This can lead to excessive power dissipation. Additionally, the load that these converters supply must be limited below the combined full load capability of the individual channel.

Without the capability to share the load current, each converter channel provides a current proportional to the average phase voltage and the net converter resistance. The average phase voltage is approximated by:

$$V_{PH} = (V_{IN} - V_{UP})D - V_{LOW}(1-D)$$

where:

$V_{IN}$ is the input voltage,
$V_{UP}$ is the voltage drop across the upper switch,
$V_{LOW}$ is the voltage across the lower switch, and
D is the duty cycle.

The net converter resistance includes the summation of the inductor winding resistance, any trace resistance, and the time multiplexed resistance of the upper and lower power switches.

In multi-phase converters, the ability to equally share the load current depends upon the matching of parameters and components between each of the phases or channels. Current sharing is particularly sensitive to any duty cycle mismatch between channels. Matching the duty cycle of multiple phases is difficult because of inherent component mismatches that can induce timing errors. As a result, any channel may be forced to carry significantly more than its

proportional share of the load current. For example, in a four-phase converter with four converter channels, one channel may carry 40% of the load current while the other channels each carry 20%, rather than each channel carrying the ideal 25%. Thus, each channel must be sized to carry at least 40% of the projected output current, or 15% more than its proportionate share. Designing each of the four channels for 40% of the projected output current, rather than for 25% of the projected output current, requires the use of oversized power output transistors and passive components, such as, for example, inductors and resistors, in order for each channel to safely conduct a higher proportion of load current. Since the distribution of the load varies, each power transistor must be larger than needed for the total load. However, if the load is more evenly distributed smaller transistors as well as smaller passive components can be used to achieve the same load current capability as oversized prior art systems. Smaller transistor and passive components are less expensive and more efficient than larger, higher-power components.

Therefore, what is needed in the art is a multi-phase converter which equally shares the load current between each of the phases or channels.

Furthermore, what is needed in the art is a multi-phase converter which uses smaller transistors and smaller passive components to produce a given load current capability, thereby making it less expensive to produce and sell.

## SUMMARY OF THE INVENTION

The present invention provides an apparatus and method for balancing the channel currents in a multi-phase DC/DC converter.

The invention comprises, in one form thereof, a multi-phase DC/DC converter having an output voltage and including a plurality of converter channels. Each converter channel includes a converter channel input and a converter channel output. Each converter channel is configured for generating a converter channel current and for adjusting said converter channel current in response to a control signal electrically connected to each converter channel input. A control circuit generates an error signal representative of a comparison of the converter output voltage to a reference voltage. The control circuit includes a plurality of control circuit channels, each of which correspond to a converter channel. Each control circuit channel generates a channel current signal representative of a corresponding converter channel current, and generates a differential channel current signal representative of a comparison of the channel current signal to an average current signal. The average current signal is representative of an overall average current for the converter channels. Each control circuit channel generates a differential error signal representative of a comparison of the error signal to the differential channel current signal. Each control circuit channel includes a pulse width modulator having a ramp input and a control input. The control input is electrically connected to the differential error signal. The pulse width modulator generates the control signal based upon the differential error signal. The control signal is electrically coupled to a corresponding converter channel input. The control circuit generates the average current signal.

## BRIEF DESCRIPTION OF THE DRAWINGS

The above-mentioned and other features and advantages of this invention, and the manner of attaining them, will become apparent and be better understood by reference to

the following description of one embodiment of the invention in conjunction with the accompanying drawings, wherein:

FIG. 1 is a block diagram of a four-phase, four-channel converter; and

FIG. 2 shows the control circuit for the four-channel converter system in FIG. 1.

Corresponding reference characters indicate corresponding parts throughout the several views. The exemplification set out herein illustrates one preferred embodiment of the invention, in one form, and such exemplification is not to be construed as limiting the scope of the invention in any manner.

## DETAILED DESCRIPTION OF THE DRAWINGS

Generally, the multi-phase converter of the present invention has multiple converter channels to source the load current. Each converter channel can be considered as an independent converter, and is controlled by a pulse-width modulated (PWM) signal. For this discussion, each converter channel is a buck converter or synchronous-rectified buck converter. The converters may share a common output capacitance.

Referring now to the drawings, and particularly to FIG. 1, there is shown one embodiment of a 4-channel multi-phase converter 10 of the present invention. Converter 10 drives load 12 and includes control circuit 14. Interconnected electrically between load 12 and control circuit 14 are, for example, four synchronous-rectified buck channels or converter channels 18a, 18b, 18c, 18d. More particularly, each converter channel 18a, 18b, 18c, 18d includes a respective converter channel input 22a, 22b, 22c, 22d. Control circuit 14 includes four control circuit outputs 14a, 14b, 14c, 14d, each of which are electrically connected to a respective one of converter channel inputs 22a, 22b, 22c, 22d. Each converter channel 18a, 18b, 18c, 18d further includes a respective converter channel output 24a, 24b, 24c, 24d, through which flows a respective converter channel current. Control circuit 14 provides at each output 14a, 14b, 14c, 14d, a separate and independent PWM signal, PWM1, PWM2, PWM3, PWM4, to each converter channel input 22a, 22b, 22c, 22d. The four PWM signals regulate the current flowing through each converter channel output 24a, 24b, 24c, 24d.

As will be described more particularly hereinafter, the output currents of converter channels 18a, 18b, 18c, 18d, are separately and individually fed back to control circuit 14. The individual PWM signals PWM1, PWM2, PWM3, PWM4 at each control circuit output 14a, 14b, 14c, 14d, respectively, are modified based at least in part upon the fed-back converter channel current. The modified or adjusted individual PWM signals PWM1, PWM2, PWM3, PWM4 are provided to each converter channel input 22a, 22b, 22c, 22d. More particularly, control circuit 14 includes current feedback lines 28a, 28b, 28c, 28d which electrically connect a respective one of converter channel outputs 24a, 24b, 24c, 24d to a respective one of control circuit inputs 32a, 32b, 32c, 32d. Thus, each of current feedback lines 28a, 28b, 28c, 28d provide a current feedback path for each of the converter channel currents flowing through converter channels 18a, 18b, 18c, and 18d, respectively. Each of feedback lines 28a, 28b, 28c, 28d, are considered as forming a part of four separate control circuit channels.

It is preferred to use a feedback method that provides a separate feedback signal from each of converter channels 18a, 18b, 18c, 18d to each control circuit channel. The separate feedback signals are each proportional to the con-

verter channel current being sourced by a corresponding converter channel. The operation of each channel 18a, 18b, 18c, 18d is then individually and separately adjusted on the basis of the fed-back converter channel current to balance the converter channel currents relative to each other. Providing to each control circuit channel a feedback signal that is proportional to the current being sourced by a corresponding converter channel eliminates issues with component mismatch between the converter channels. Generally, and as will be described with more particularity hereinafter, converter 10 subtracts from an error amplifier's output a signal that is proportional to the converter current imbalance existing between the converter channels to thereby correct for any imbalance between the converter currents.

Feed back path 34 electrically connects output 36 of converter 10 to feedback input 32f of control circuit 14. Control circuit 14 thus receives via feed back path 34 the voltage being supplied to load 12.

Referring now to FIG. 2, control circuit 14 is shown in more detail. Generally, and as will be described with more particularity hereinafter, the converter channel current of each converter channel 18a, 18b, 18c, 18d is individually compared to the overall average converter channel current of all the converter channels 18a, 18b, 18c, and 18d. The current of each converter channel 18a, 18b, 18c, 18d is then individually and separately adjusted to bring it closer to the average and, therefore, making the converter channel current in each of converter channels 18a, 18b, 18c, 18d substantially equal to each other.

Error amplifier (E/A) 42 has a first input 32f electrically connected via feedback path 34 to output 36 of converter 10. E/A 42 compares the voltage at converter output 36, or the load voltage, to a reference voltage REF electrically connected to input 42a of error amplifier 42. The output voltage $VE/A$ appearing on output 42b of E/A 42 increases when the voltage at output 36 of converter 10 is below the reference voltage applied to input 42a of E/A 42. Conversely, the output voltage VE/A appearing on output 42b of E/A 42 decreases when the voltage at output 36 of converter 10 is above the reference voltage applied to input 42a of E/A 42. The current flowing from each converter channel output 24a, 24b, 24c, 24d flows through a series resistor (not shown) in each of current feedback paths 28a, 28b, 28c, 28d to thereby create $V_{ISENSE1}$, $V_{ISENSE2}$, $V_{ISENSE3}$, and $V_{ISENSE4}$, respectively. Each of $V_{ISENSE1}$, $V_{ISENSE2}$, $V_{ISENSE3}$, and $V_{ISENSE4}$, is proportional to the individual converter channel current flowing through converter channel outputs 24a, 24b, 24c, 24d, respectively. Each of $V_{ISENSE1}$, $V_{ISENSE2}$, $V_{ISESNE3}$, and $V_{ISENSE4}$, is electrically connected to control circuit 14 via feedback paths 28a, 28b, 28c, 28d, respectively. However, it is to be understood that the series resistor may be integrated within control circuit 14, in which case feedback paths 28a, 28b, 28c, 28d would deliver the converter channel currents flowing through converter channel outputs 24a, 24b, 24c, 24d, respectively, and in which case $V_{ISENSE1}$, $V_{ISENSE2}$, $V_{ISENSE3}$, and $V_{ISENSE4}$ would be created internally of control circuit 14.

Summing circuit 44 includes inputs 44a, 44b, 44c, 44d, each of which are electrically connected to control circuit inputs 32a, 32b, 32c, 32d, thereby connecting inputs 44a, 44b, 44c, 44d of summing circuit 44 to $V_{ISENSE1}$, $V_{ISENSE2}$, $V_{ISENSE3}$, $V_{ISENSE4}$, respectively. Summing circuit 44 adds together each of $V_{ISENSE1}$, $V_{ISENSE2}$, $V_{ISENSE3}$, and $V_{ISENSE4}$, and produces a signal proportional to the sum of $V_{ISENSE1}$, $V_{ISENSE2}$, $V_{ISENSE3}$, and $V_{ISENSE4}$ at output 44f. Output 44f of summing circuit 44 is electrically connected to input 46a of scaling circuit 46. Scaling circuit 46 scales (i.e.,

divides by 4) the sum of $V_{ISENSE1}$, $V_{ISENSE2}$, $V_{ISENSE3}$, and $V_{ISENSE4}$ to thereby produce signal $V_{average}$, which is proportional to the average of $V_{ISENSE1}$, $V_{ISENSE2}$, $V_{ISENSE3}$, and $V_{ISENSE4}$, at output 46b.

Each control circuit channel includes a respective subtraction circuit 48, 50, 52, 54. Each of subtraction circuits 48, 50, 52, 54 include inputs 48a and 48b, 50a and 50b, 52a and 52b, and 54a and 54b, respectively. Input 48a of subtraction circuit 48 is electrically connected to input 32a of control circuit 14, thereby connecting input 48a of subtraction circuit 48 to $V_{ISENSE1}$. Input 50a of subtraction circuit 50 is electrically connected to input 32b of control circuit 14, thereby connecting input 50a of subtraction circuit 48 to $V_{ISENSE2}$. Input 52a of subtraction circuit 52 is electrically connected to input 32c of control circuit 14, thereby connecting input 52a of subtraction circuit 48 to $V_{ISENSE2}$. Likewise, input 54a of subtraction circuit 54 is electrically connected to input 32d of control circuit 14, thereby connecting input 54a of subtraction circuit 48 to $V_{ISENSE4}$. Each input 48b, 50b, 52b, and 54b of subtraction circuits 48, 50, 52, 54, respectively, is electrically connected to output 46b of scaling circuit 46, thereby connecting each input 48b, 50b, 52b, 54b to $V_{average}$. Each of the subtraction circuits 48, 50, 52, 54, subtracts $V_{average}$ from each of $V_{ISENSE1}$, $V_{ISENSE2}$, $V_{ISENSE3}$, and $V_{ISENSE4}$. More particularly, subtraction circuit 48 subtracts $V_{average}$ from $V_{ISENSE1}$, subtraction circuit 50 subtracts $V_{average}$ from $V_{ISENSE2}$, subtraction circuit 52 subtracts $V_{average}$ from $V_{ISENSE3}$, and subtraction circuit 54 subtracts $V_{average}$ from $V_{ISENSE4}$. The results of the subtraction performed by each of subtraction amplifiers 48, 50, 52, 54 represent the difference between the current flowing through a respective one of converter channels 18a, 18b, 18c, 18d and the average of the converter channel currents being sourced conjunctively by converter channels 18a, 18b, 18c, 18d (i.e., the value represented by $V_{average}$). Outputs 48c, 50c, 52c, and 54c of subtraction circuits 48, 50, 52, 54, respectively, are electrically connected to a respective one of compensation circuits G.

Each control circuit channel also includes a compensation circuit G1, G2, G3, G4. Each compensation circuit G1, G2, G3, G4 performs current loop compensation functions, such as, for example, gain or filter functions to shape the current feedback wave, to achieve adequate current balancing, or to prevent current loop instability. Each compensation circuit G1, G2, G3, G4 may include at least one pole and zero. The output of each compensation circuit G1, G2, G3, G4 represents the difference between the current flowing through a respective one of converter channels 18a, 18b, 18c, 18d and the overall average of the converter channel currents being sourced conjunctively by converter channels 18a, 18b, 18c, 18d (i.e., the value represented by $V_{average}$), and is represented by signals $\Delta I_1$, $\Delta I_2$, $\Delta I_3$, $\Delta_4$, respectively. Thus, signals $\Delta I_1$, $\Delta I_2$, $\Delta I_3$, $\Delta I_4$ represent the difference between the overall average of the converter channel currents being sourced conjunctively by converter channels 18a, 18b, 18c, 18d (i.e., the value represented by $V_{average}$) and the actual value of the current flowing within converter channels 18a, 18b, 18c, and 18d, respectively. More particularly, and for example, $\Delta I_1$ represents the difference between the overall average of the converter channel currents being sourced conjunctively by channels 18a, 18b, 18c, 18d, and the actual value of the converter channel current flowing within converter channel 18a. Likewise, and as a further example, $\Delta I_2$ represents the difference between the overall average of the converter channel currents being sourced conjunctively by converter channels 18a, 18b, 18c, 18d, and the actual value

of the current flowing within converter channel 18b. Ideally, each of the $\Delta I_1$, $\Delta I_2$, $\Delta I_3$, and $\Delta I_4$ signals will be zero, thus indicating equal converter channel currents are flowing through each of converter channels 18a, 18b, 18c, 18d. Signals $\Delta I_1$, $\Delta I_2$, $\Delta I_3$, $\Delta I_4$ are input into subtraction circuits 58, 60, 62, 64, respectively.

Each control circuit channel includes a subtraction circuit 58, 60, 62, 64. Each of subtraction circuits 58, 60, 62, 64 include respective inputs 58a and 58b, 60a and 60b, 62a and 62b, and 64a and 64b. Inputs 58a, 60a, 62a, and 64a are electrically connected to G1, G2, G3, and G4, respectively, thereby connecting each of subtraction circuits 58, 60, 62, and 64 to signals $\Delta I_1$, $\Delta I_2$, $\Delta I_3$, $\Delta I_4$, respectively. Each of inputs 58b, 60b, 62b, and 64b, are electrically connected to output 42b of E/A 42, thereby connecting each subtraction circuit 58, 60, 62, and 64 to VE/A. As described hereinabove, VE/A increases when the voltage at output 36 of converter 10 is below the reference voltage REF applied to input 42a of E/A 42. Conversely, the output voltage VE/A of output 42b decreases when the voltage at output 36 of converter 10 is above the reference voltage REF applied to input 42a of E/A 42. Difference or subtraction circuits 58, 60, 62, and 64 compare a respective one of $\Delta I_1$, $\Delta I_2$, $\Delta I_3$, and $\Delta I_4$ to signal VE/A. Outputs 58c, 60c, 62c, and 64c of subtraction circuits 58, 60, 62, 64, respectively, are electrically connected to a respective one of PWM amplifiers 68, 70, 72, 74.

Each control circuit channel includes a PWM amplifier 68, 70, 72, 74. Each of PWM amplifiers 68, 70, 72, 74 include inputs 68a and 68b, 70a and 70b, 72a and 72b, and 74a and 74b, respectively. Inputs 68a, 70a, 72a, 74a are electrically connected to outputs 58c, 60c, 62c, 64c, respectively, of subtraction circuits 58, 60, 62, 64, respectively. Each input 68b, 70b, 72b, 74b is connected to a reference PWM waveform. PWM amplifiers 68, 70, 72, 74 modify the reference PWM waveform dependent at least in part upon inputs 68a, 70a, 72a, 74a, respectively. More particularly, the pulse width of the reference PWM will be individually and separately modified by each PWM amplifier 68, 70, 72, 74 dependent at least in part upon a respective one of inputs 68a, 70a, 72a, 74a. The individually and separately modified reference PWM waveforms appear at control circuit outputs 14a, 14b, 14c, 14d of PWM amplifiers 68, 70, 72, 74, respectively, as signal PWM1, PWM2, PWM3, and PWM4, respectively. The modification of the reference PWM waveform by each PWM amplifier 68, 70, 72, and 74 is in such a direction as to bring the converter channel current of each converter channel 18a, 18b, 18c, 18d closer to the average output current, $V_{average}$. More particularly, the pulse width of each of signals PWM1, PWM2, PWM3, PWM4, will be modified (i.e. shortened or lengthened) in such a direction as to bring the converter channel current of each converter channel 18a, 18b, 18c, 18d closer to the average output current, $V_{average}$. Each signal PWM1, PWM2, PWM3, and PWM4 of PWM amplifiers 68, 70, 72, 74, respectively, is electrically connected to a respective one of converter channel inputs 22a, 22b, 22c, and 22d, respectively, as described hereinabove.

In use, when converter 10 is operating under, for example, the condition that converter channel 18a is carrying a converter channel current that is higher than the average of all converter channel currents, as represented by $V_{average}$, subtraction circuit 48 will generate a positive $\Delta I_1$ signal. This positive $\Delta I_1$ is input into subtraction circuit 58. Subtraction circuit 58 subtracts the positive $\Delta I_1$ signal from VE/A, i.e. the output of error amplifier 42, thereby reducing output 58c, which is electrically connected to input 68a of